WHAT IS CLAIMED IS:

1. A method for converting a signal from a low voltage domain to a high voltage domain, comprising:

receiving an input signal in a low voltage domain; and

using the input signal, controlling a first transistor having a first carrier type, a second transistor having a second carrier type different from the first carrier type, and a third transistor having the second carrier type to produce an output voltage at an output terminal, wherein:

the first transistor is coupled to the output terminal and further coupled to a first voltage corresponding to a first value in a high voltage domain;

the second and third transistors are coupled in series between the output terminal and a second voltage corresponding to a second value in the high voltage domain; and

the output voltage is selected to correspond to either the first voltage or the second voltage based upon the input signal.

2. The method of Claim 1, further comprising amplifying the output voltage by an amount of voltage less than the difference between the maximum values of the high and low voltage domains by at least a factor of two.

3. The method of Claim 1, wherein:

the input signal is received at a logical gate operable to apply a logical operation to the input signal; and

the method further comprises applying the logical operation of the logical gate to the input signal before the transistors are controlled using the input signal.

4. The method of Claim 1, wherein:

the high value of the low voltage domain is 1.25 volts; and

the high value of the high voltage domain is 2.5 V.

5. The method of Claim 1, wherein the step of controlling comprises applying the input signal to at least one control transistor operable to control at least one of the second and third transistors.

6. The method of Claim 5, wherein the method further comprises:

dividing the input signal into two portions, wherein the first portion of the input signal is applied to the control transistor;

inverting the second portion of the input signal; and

applying the second portion of the input signal to a gate terminal of the first transistor.

7. The method of Claim 1, wherein the input signal has a frequency greater than 1 gigahertz.

8. A circuit for converting a signal from a low voltage domain to a high voltage domain, comprising:

a receiver operable to receive an input signal in a low voltage domain; and

a first transistor having a first carrier type, wherein the first transistor is coupled to the output terminal and further coupled to a first voltage corresponding to a first value in a high voltage domain;

a second transistor having a second carrier type different from the first carrier type;

a third transistor having the second carrier type, wherein the second and third transistors are coupled in series between the output terminal and a second voltage corresponding to a second value in the high voltage domain; and

a control structure operable to control the first, second, and third transistors to produce an output at the output terminal corresponding to either the first voltage or the second voltage in response to the input signal.

9. The circuit of Claim 8, further comprising an output amplifier operable to amplify the output voltage by an amount of voltage less than the difference between the maximum values of the high and low voltage domains by at least a factor of two.

10. The circuit of Claim 8, wherein the receiver comprises a logical gate operable to apply the operation of the logical gate to the input signal.

11. The circuit of Claim 8, wherein:

the high value of the low voltage domain is 1.25 volts; and

the high value of the high voltage domain is 2.5 V.

12. The circuit of Claim 8, wherein the control structure comprises at least one control transistor operable to control at least one of the second and third transistors.

13. The circuit of Claim 12, wherein:

the receiver is further operable to divide the input signal into two portions;

the control structure is further operable to apply the first portion of the input signal to the control transistor;

the control structure further comprises an inverter operable to invert the second portion of the input signal; and

the control structure is further operable to apply the second portion of the input signal to a gate terminal of the first transistor.

14. The circuit of Claim 8, wherein the input signal has a frequency greater than 1 gigahertz.

15. A circuit for converting a signal from a low voltage domain to a high voltage domain, comprising:

means for receiving an input signal in a low voltage domain; and

means for controlling a first transistor, a second transistor, and a third transistor to produce an output voltage at an output terminal using the input signal, the first transistor having a first carrier type, the second transistor having a second carrier type different from the first carrier type, and the third transistor having the second carrier type, wherein:

the first transistor is coupled to the output terminal and further coupled to a first voltage corresponding to a first value in a high voltage domain;

the second and third transistors are coupled in series between the output terminal and a second voltage corresponding to a second value in the high voltage domain; and

the output voltage is selected to correspond to either the first voltage or the second voltage based upon the input signal.

16. The circuit of Claim 15, further comprising means for amplifying the output voltage by an amount of voltage less than the difference between the maximum values of the high and low voltage domains by at least a factor of two.

17. The circuit of Claim 15, further comprising means for applying the logical operation to the input signal before the transistors are controlled by the controlling means.

18. A circuit for converting from a low voltage domain to a high voltage domain, comprising:

an inverted NAND gate;

an inverter coupled to the inverted NAND gate;

a first transistor having a first carrier type, the first transistor coupled to a high voltage corresponding to a high value in a high voltage domain and further coupled to an output terminal and to the inverter at a gate terminal of the first transistor;

a second transistor having a second carrier type different from the first carrier type coupled to the output terminal;

a third transistor having the second carrier type coupled in series with the second transistor between the output terminal and a low voltage corresponding to a low value in the high voltage domain;

a fourth transistor coupled to the inverter at a gate terminal of the fourth transistor and further coupled to a gate terminal of the third transistor; and

a fifth transistor coupled to the inverted NAND gate at a gate terminal of the fifth transistor and further coupled to the second voltage and the gate terminal of the third transistor.

19. The circuit of Claim 18, wherein:

the first, second, third, fourth, and fifth transistors are all metal oxide semiconductor field effect transistors (MOSFETs);

the first and fourth transistors are positive carrier type MOSFETs; and

the second, third, and fifth transistors are negative carrier type MOSFETs.

20. The circuit of Claim 18, further comprising an output amplifier operable to amplify the output voltage by an amount substantially less than the difference between the maximum values of the high and low voltage domains.